2

1

IN THE CLAIMS

What is claimed is:

	1
M, K)	$)_2$
(1)	3
•	4
	5
1	1
*.j	
	2
<u>u</u> j	_
	3
	-
<u>1_1</u>	

An integrated circuit device, comprising:

a programmable portion comprising a plurality of circuits that may be configured by a user of the integrated circuit device; and

at least one communication portion comprising at least one circuit block manufactured to perform a predetermined data communication function.

2. The integrated circuit device of claim 1, wherein:

the programmable portion comprises a programmable interconnect portion and a logic gate portion.

1 3. The integrated circuit device of claim 2, further including:

a memory circuit for storing configuration information for configuring circuits of the programmable portion.

4. The integrated circuit device of claim 2, further including:

a timing circuit that receives a clock signal and generates an internal clock signal that is phase shifted with respect to the clock signal.

- 1 5. The integrated circuit device of claim 1, further including:
- a plurality of input/outputs commonly connected to the programmable

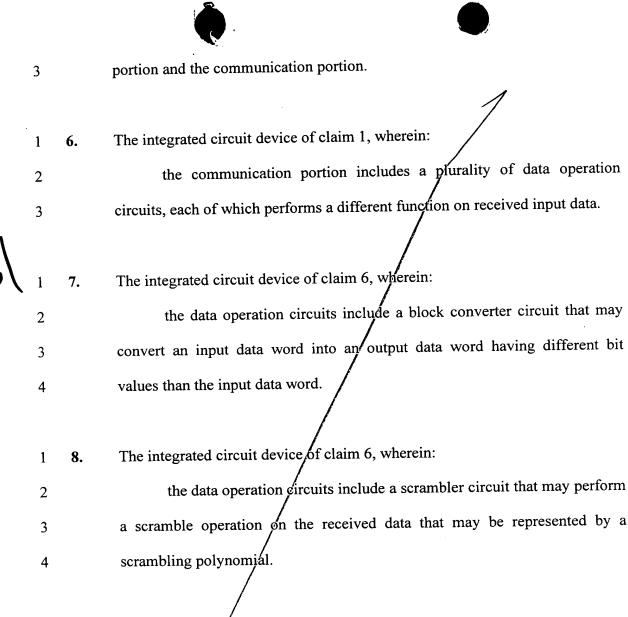
1

2

3

4

2



9. The integrated circuit device of claim 6, wherein:

the communication portion further includes an operation control store that provides one of a plurality of operational values to the data operation circuits that controls the type of operation performed on the received data.

1 10. The integrated circuit device of claim 9, wherein:

the data operation circuits include a scrambler circuit that may perform



		<i>-</i>
3		a scramble operation on the received data; and
4		the operation control store provides operational values that represent at
5		least one scrambling polynomial.
1	11.	The integrated circuit device of claim 9, wherein:
2		the operational control store includes circuits that may provide at least
3		one user operational value configured by a user and preset operational values
4		that may be established by at least one integrated circuit manufacturing step.
1	12.	The integrated circuit device of claim 6, wherein:
2		the communication portion includes a data (MUX) multiplexer that
3		enables a data path between one of a plurality of inputs and a data MUX
4		output, and each data operation circuit is coupled to an input of the data MUX
1	13.	The integrated circuit device of claim 6, wherein:
2		the communication portion includes a physical layer circuit tha
3		provides a data output stream compatible with a particular data transmission
4		media.
1	14.	The integrated circuit device of claim 6, wherein:

- the at least one communication portion includes a plurality of
- 3 communication portions.

2

1	15.	A semiconductor device, comprising:
2		a programmable logic device having a communication portion
3		embedded therein, the communication portion including non-programmable
4		circuits designed to provide a selectable data communication function.
1	16.	The semiconductor device of claim 15, wherein:
2		the communication portion includes a plurality of circuit blocks that
3		each provides a different data communication function.
1	17.	The semiconductor device of claim 16, wherein:
2		the communication portion includes a selectable data path between
3		each circuit block and a data output.
1	18.	The semiconductor device of claim 15, wherein:
2		the communication portion includes a block converter circuit that
3		encodes input data words into output data words and a scrambler circuit that
4		scrambles data values according to an operational control value.
1	19.	The semiconductor device of claim 15, wherein:
2	•	the communication portion includes a block converter circuit that
3		decodes input data words into output data words and a de-scrambler circuit
4		that de-scrambles data values according to an operational control value.



3.

20. The semiconductor device of claim 18, wherein:

the communication portion includes an operational control store that

provides selectable operational control values to the scrambler circuit.

	1
	\
e ļul	

Sign		21.)	A method, comprising the steps of:
0,	2		performing predetermined logic functions on a programmable logic
	3		portion of the integrated circuit; and
	4		performing serial data communication functions on a communication
	5		portion of the integrated circuit that includes circuit blocks that are not
	6		synthesized.
			_
	1	22.	The method of claim 21, wherein:
.	2		performing serial data communication functions includes
	3		selecting a polynomial value from a number of polynomial
1	4		values, and
/	5		scrambling serial data according to the selected polynomial
	6		value.
	1	23.	The method of claim 21, wherein:
	2		performing serial data communication functions includes encoding
	3		serial data having words of a first bit length into serial data having words of a
	4		second bit length that is different than the first bit length.